WHAT IS CLAIMED IS

1. A method comprising:

detecting a first level cache does not contain branch prediction information corresponding to a first address;

determining whether a second level cache contains branch prediction information corresponding to said first address;

rebuilding a first branch prediction using said information in response to determining said second level cache contains said information, wherein said information comprises a subset of said first branch prediction; and

storing said first branch prediction in a first entry of said first level cache, wherein said first entry corresponds to said first address.

2. The method of claim 1, further comprising:

determining if said first entry of said first level cache is available;

evicting contents of said first entry in response to detecting said first entry is not available; and

storing a subset of said contents in said second level cache responsive to said eviction.

3. The method of claim 1, wherein said branch prediction corresponds to a first branch instruction, and wherein said branch prediction further comprises information indicating a type of said branch instruction.

4. The method of claim 3, wherein rebuilding said first branch prediction comprises decoding said branch instruction.

5. The method of claim 4, wherein said branch instruction is fetched from said second level cache.

6. The method of claim 1, wherein said subset comprises a dynamic bit.

7. The method of claim 6, wherein said subset further comprises a branch marker bit.

8. The method of claim 7, wherein said branch prediction further comprises an end adjustment bit.

9. A branch prediction mechanism comprising:

a first level cache configured to store branch prediction information;

a second level cache configured to store branch prediction information;

circuitry coupled to said first level cache and said second level cache, wherein said circuitry is configured to detect said first level cache does not contain branch prediction information corresponding to a first address, determine whether said second level cache contains branch prediction information corresponding to said first address, rebuild a first branch prediction using said information in response to determining said second level cache contains said information, wherein said information comprises a subset of said first branch prediction, and store said first branch prediction in a first entry of said first level cache, wherein said first entry corresponds to said first address.

10. The mechanism of claim 9, wherein said circuitry is further configured to:

determine if said first entry of said first level cache is available;

evict contents of said first entry in response to detecting said first entry is not available; and

store a subset of said contents in said second level cache responsive to said eviction.

11. The mechanism of claim 9, wherein said branch prediction corresponds to a first branch instruction, and wherein said branch prediction further comprises information indicating a type of said branch instruction.

12. The mechanism of claim 11, wherein rebuilding said first branch prediction comprises decoding said branch instruction.

13. The mechanism of claim 12, wherein said branch instruction is fetched from said second level cache.

14. The mechanism of claim 9, wherein said subset comprises a dynamic bit.

15. The mechanism of claim 14, wherein said subset further comprises a branch marker bit.

16. The mechanism of claim 15, wherein said branch prediction further comprises an end adjustment bit.

17. A computer system comprising:

an interconnect;

a memory coupled to said interconnect;

a second level cache configured to store branch prediction information;

a processor including a first level cache, wherein said processor is configured to:

detect said first level cache does not contain branch prediction information corresponding to a first address,

determine whether said second level cache contains branch prediction information corresponding to said first address,

rebuild a first branch prediction using said information in response to determining said second level cache contains said information, wherein said information comprises a subset of said first branch prediction, and

store said first branch prediction in a first entry of said first level cache, wherein said first entry corresponds to said first address.

18. The system of claim 17, wherein said processor is further configured to determine if said first entry of said first level cache is available; evict contents of said first entry in response to detecting said first entry is not available; and store a subset of said contents in said second level cache responsive to said eviction.

19. The system of claim 17, wherein said branch prediction corresponds to a first branch instruction, and wherein said branch prediction further comprises information indicating a type of said branch instruction.

20. The system of claim 19, wherein rebuilding said first branch prediction comprises decoding said branch instruction.